REMARKS

This Response responds to a Final Office Action dated June 19, 2003, in the above-identified patent application. Claims 1-17 are currently pending.

This Response is being filed within three months of the Final Office Action outstanding. No claims have been added or amended. No additional claim fees or time extension fees are required.

In the Final Office Action dated June 19, 2003, the Examiner rejected claims 1-17 under 35 USC §112, first paragraph, as allegedly failing to comply with the written description requirement. The Examiner stated: "It appears that the specification does not have support for a method or an apparatus for exercising, connecting and optically stimulating components on the integrated circuit simultaneously as recited in [the] recently amended claims. From the specification, it appears that there is only one component on an integrated circuit [that] is exercised, connected to an electrical source and optically stimulated one at a time."

Applicant respectfully disagrees. Applicant's specification does have support for exercising, connecting and optically stimulating components on an integrated circuit simultaneously, as recited in the recently amended claims. In particular, Applicant's specification as originally filed at page 22, lines 5-7 recites: "In the preferred embodiment, probe card 74 extends across the full diameter 12 of wafer 10 so that a single probe card is used during

simultaneous burn-in of each die on the wafer." Applicant's specification as originally filed at page 18, line 23 through page 19, line 2 recites: "In the embodiment shown, individual fiber optic strands 92 [of fiber optic block 70] are densely packed so that bundle 90 extends across the entire diameter of chamber 60 and, therefore, across the entire diameter 12 of wafer 10." Applicant's specification as originally filed at page 23, lines 5-6 recites: "Accordingly, switch 120 is the main control switch for simultaneously providing power to each die on wafer 10." Applicant's specification as originally filed at page 23, lines 9-11 recites: "Utilizing switch 121 to isolate an individual die reduces the problem of one die shorting out the power to all other die on the wafer when all the die are electrically tested in parallel." Applicant's specification as originally filed at page 24, lines 12-14 recites: "Lead 132 is electrically connected to metallic signal source layer 114 so that each of the die on wafer 10 is electrically connected in parallel to the signal layer." Applicant's specification as originally filed at page 28, lines 20-21 recites: "The portion of probe card 74 shown in Fig. 11 includes optical switch 120 for simultaneously powering on and off all the die on the wafer."

There is ample support in the specification for a method and an apparatus for exercising, connecting and optically stimulating components on an integrated circuit simultaneously as recited in the recently amended claims. Applicant requests, therefore, that the Examiner withdraw the rejection of claims 1-17 under 35 USC 112, first paragraph.

There are no other rejections of the claims. In view of the foregoing, applicant requests reconsideration of the application and submits that the application is fully allowable and should be passed to issue.

Respectfully submitted,

Date: September 10, 2003

David C. Ripma
Registration No. 27,672

David C. Ripma, Patent Counsel
Sharp Laboratories of America, Inc.
5750 N.W. Pacific Rim Blvd.
Camas, WA 98607

Telephone: (360) 834-8754
Facsimile: (360) 817-8505